Appendix A: Model Instance Syntax

```
Mname <D node> <G node> <S node> <E node> [P node]
      [B node] [T node] <model>
      [L=<val>] [W=<val>]
      [AD=<val>] [AS=<val>] [PD=<val>] [PS=<val>]
      [NRS=<val>] [NRD=<val>] [NRB=<val>]
      [OFF][BJTOFF=<val>]
      [IC=<val>,<val>,<val>,<val>,<val>]
      [RTH0=<val>] [CTH0=<val>]
      [DEBUG=<val>]
      [DELVTO=<val>]
      [SA=<val>][SB=<val>][SD=<val>]
      [NF=<val>]
      [NBC=<val>] [NSEG=<val>] [PDBCP=<val>] [PSBCP=<val>]
      [AGBCP=<val>][AEBCP=<val>][VBSUSR=<val>][TNODEOUT]
      [FRBODY=<val>][AGBCPD=<val>]
```

A.1. Description

<D node>	Drain node
<G node>	Gate node
<S node>	Source node
<E node>	Substrate node
[P node]	(Optional) external body contact node
[B node]	(Optional) internal body node
[T node]	(Optional) temperature node
<model>	Level 9 BSIM3SOI model name
[L]	Channel length
[W]	Channel width

[AD]	Drain diffusion area
[AS]	Source diffusion area
[PD]	Drain diffusion perimeter length
[PS]	Source diffusion perimeter length
[NRS]	Number of squares in source series resistance
[NRD]	Number of squares in drain series resistance
[NRB]	Number of squares in body series resistance
[OFF]	Device simulation off
[BJTOFF]	Turn off BJT current if equal to 1
[IC]	Initial guess in the order of (Vds, Vgs, Vbs, Ves, Vps). (Vps will be ignored in the case of 4-terminal device)
[RTH0]	Thermal resistance per unit width ■ if not specified, RTH0 is extracted from model card. ■ if specified, it will override the one in model card.
[CTH0]	Thermal capacitance per unit width ■ if not specified, CTH0 is extracted from model card. ■ if specified, it will over-ride the one in model card.
[DEBUG]	Please see the debugging notes
[DELVTO]	Zero bias threshold voltage variation
[SA]	Stress effect parameter
[SB]	Stress effect parameter
[SD]	Stress effect parameter
[NF]	Number of fingers
[NBC]	**Number of body contact isolation edge**
[NSEG]	**Number of segments for channel width partitioning [17]**
[PDBCP]	**Parasitic perimeter length for body contact at drain side**
[PSBCP]	**Parasitic perimeter length for body contact at source side**
[AGBCP]	**Parasitic gate-to-body overlap area for body contact**
[AEBCP]	**Parasitic body-to-substate overlap area for body contact**
[VBSUSR]	**Optional initial value of Vbs specified by user for transient analysis**

[TNODEOUT] **Temperature node flag indicating the usage of T node**

[FRBODY] **Layout-dependent body resistance coefficient**

[AGBCPD] **Parasitic gate-to-body overlap area for body contact in DC**

A.2. About Optional Nodes

There are three optional nodes, P, B and T nodes. P and B nodes are used for body contact devices. Let us consider the case when TNODEOUT is not set. If user specifies four nodes, this element is a 4-terminal device, i.e., floating body. If user specifies five nodes, the fifth node represents the external body contact node (P). There is a body resistance between internal body node and P node. In these two cases, an internal body node is created but it is not accessible in the circuit deck. If user specifies six nodes, the fifth node represents the P node and the sixth node represents the internal body node (B). This configuration is useful for distributed body resistance simulation.

If TNODEOUT flag is set, the last node is interpreted as the temperature node. In this case, if user specifies five nodes, it is a floating body case. If user specifies six nodes, it is a body-contacted case. Finally, if user specifies seven nodes, it is a body-contacted case with an accessible internal body node. The temperature node is useful for thermal coupling simulation.

A.3. Notes on Debugging

The instance parameter <DEBUG> allows users to turn on debugging information selectively. Internal parameters (e.g. par) for an instance (e.g. m1) can be plotted by this command:

plot m1#par

By default, <DEBUG> is set to zero and two internal parameters will be available for plotting:

#body	V_b value iterated by SPICE
#temp	Device temperature with self-heating mode turned on

If <DEBUG> is set to one or minus one, more internal parameters are available for plotting. This serves debugging purposes when there is a convergence problem. This can also help the user to understand the model more. For <DEBUG> set to minus one, there will be charge calculation even if the user is running DC simulation. Here is the list of internal parameters:

#Vbs	Real V_{bs} value used by the IV calculation
#Vgsteff	Effective gate-overdrive voltage
#Vth	Threshold voltage
#Ids	MOS drain current
#Ic	BJT current
#Ibs	Body to source diode current
#Ibd	Body to drain diode current
#Iii	Impact ionization current
#Igidl	GIDL current
#Itun	Tunneling current
#Ibp	Body contact current
#Gds	Output conductance
#Gm	Transconductance
#Gmb	Drain current derivative wrt Vbs

These parameters are valid only if charge computation is required

#Cbb	Body charge derivative wrt Vbs
#Cbd	Body charge derivative wrt Vds
#Cbe	Body charge derivative wrt Ves
#Cbg	Body charge derivative wrt Vgs
#Qbody	Total body charge
#Qgate	Gate charge
#Qac0	Accumulation charge
#Qsub	Bulk charge
#Qsub0	Bulk charge at zero drain bias

#Qbf	Channel depletion charge
#Qjd	Parasitic drain junction charge
#Qjs	Parasitic source junction charge