Chapter 2: MOS I-V Model

A typical PD SOI MOSFET structure is shown in Fig. 2.1. The device is formed on a thin SOI film of thickness T_{si} on top of a layer of buried oxide with thickness T_{box}. In the floating body configuration, there are four external biases which are gate voltage (V_g), drain voltage (V_d), source voltage (V_s) and substrate bias (V_e). The body potential (V_b) is iterated in circuit simulation. If a body contact is applied, there will be one more external bias, the body contact voltage (V_p).

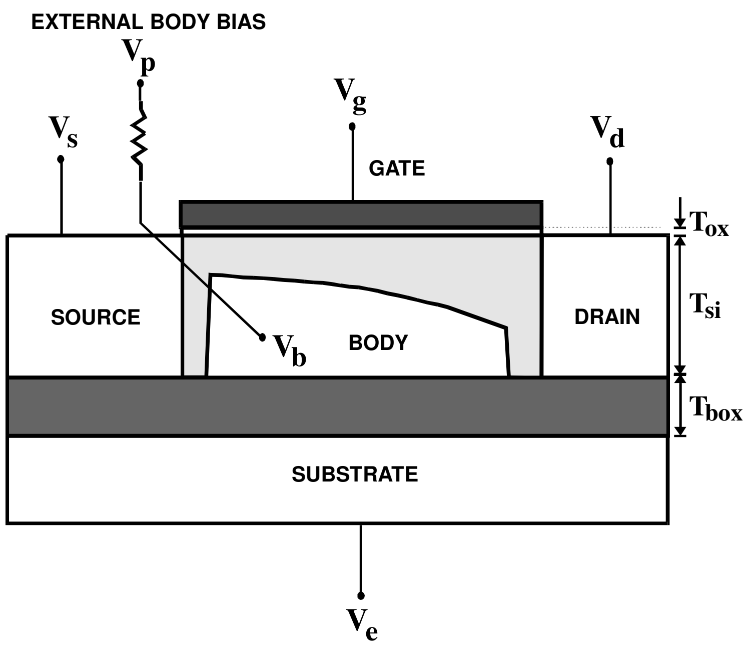

Fig. 2.1 Schematic of a typical PD SOI MOSFET.

Since the backgate (V_e) effect is decoupled by the neutral body, PD SOI MOSFETs have similar characteristics as bulk devices. Hence most PD SOI models reported [5, 6] were developed by adding some SOI specific effects onto a bulk model. These effects include parasitic bipolar current, self-heating and body contact resistance.

BSIMPD is formulated on top of the BSIM3v3 framework. In this way, a lot of physical effects which are common in bulk and SOI devices can be shared. These effects are reverse short channel effect, poly depletion, velocity saturation, DIBL in subthreshold and output resistance, short channel effect, mobility degradation, narrow width effect and source/drain series resistance [1, 4].

2.1. Floating Body Operation and Effective Body Potential

In BSIMPD, the floating body voltage is iterated by the SPICE engine. The result of iteration is determined by the body currents [7, 18]. In the case of DC, body currents include diode current, impact ionization, gate-induced drain leakage (GIDL), oxide tunneling and body contact current. For AC or transient simulations, the displacement currents originated from the capacitive coupling are also contributive.

To ensure a good model behavior during simulations, the iterated body potential V_{bs} is bounded by the following smoothing function

$$T_1 = V_{bsc} + 0.5\left[V_{bs} - V_{bsc} - \delta + \sqrt{(V_{bs} - V_{bsc} - \delta)^2 - 4\delta V_{bsc}}\right],\ V_{bsc} = -5V \tag{2.1}$$

$$V_{bsh} = \phi_{s1} - 0.5\left[\phi_{s1} - T_1 - \delta + \sqrt{(\phi_{s1} - T_1 - \delta)^2 + 4\delta T_1}\right],\ \phi_{s1} = 1.5V \tag{2.2}$$

Here the body potential V_{bsh} is equal to the V_{bs} bounded between (V_{bsc}, ϕ_{s1}), and is used in the threshold voltage and bulk charge calculation. To validate the popular square root expression $\sqrt{\phi_s - V_{bsh}}$ in the MOSFET model, V_{bsh} is further limited to $0.95\phi_s$ to give the following effective body potential

$$V_{bseff} = \phi_{s0} - 0.5\left[\phi_{s0} - V_{bsh} - \delta + \sqrt{(\phi_{s0} - V_{bsh} - \delta)^2 + 4\delta V_{bsh}}\right],\ \phi_{s0} = 0.95\phi_s \tag{2.3}$$

2.2. Threshold Voltage in the High Vbs Regime

2.2.1. Linear Extrapolation for the Square-Root Epression

Using the V_{bseff} which is clamped to the surface potential ϕ_s, the square-root dependence $\sqrt{\phi_s - V_{bseff}}$ of the threshold voltage is ensured to behave properly during simulations [20]. However the real body potential may be larger than the surface potential in state-of-the-art PD SOI technologies. To accurately count the body effect in such a high body bias regime, we extend the square-root expression by

$$sqrtPhisExt = \sqrt{\phi_s - V_{bseff}} + s\left(V_{bsh} - V_{bseff}\right), \quad s = -\frac{1}{2\sqrt{\phi_s - \phi_{s0}}} \tag{2.4}$$

where a linear extrapolation is employed for $V_{bsh} \geq 0.95\phi_s$. Notice that $sqrtPhisExt = \sqrt{\phi_s - V_{bseff}}$ for $V_{bsh} \leq 0.95\phi_s$.

2.2.2. Width Dependence of the Body Effect

In BSIMPD, the body effect coefficient K_1 is replaced by

$$K_{1eff} = K_1\left(1 + \frac{K_{1w1}}{W'_{eff} + K_{1w2}}\right) \tag{2.5}$$

to model the width dependence of the body effect. Notice that K_{1eff} approaches K_1 asymptotically as the effective channel width W'_{eff} increases. While the body effect coefficient will be determined by the parameters (K_{1w1}, K_{1w2}) when W'_{eff} becomes small so that the contribution from the channel-stop doping should be taken into account.

The complete equation of the threshold voltage V_{th} can be found in the Appendix C.

2.3. Bulk Charge Effect in the High Vbs Regime

The bulk charge factor in BSIMSOI4.0 is given as

$$A_{bulk} = 1 + \left(\frac{K_{1ox} \cdot \sqrt{1 + LPEB / L_{eff}}}{2\sqrt{(\phi_s + Ketas) - \dfrac{V_{bsh}}{1 + Keta \cdot V_{bsh}}}} \left(\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{T_{si} X_{dep}}} \left(1 - A_{gs} V_{gsteff} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{T_{si} X_{dep}}} \right)^2 \right) + \frac{B_0}{W_{eff}^{'} + B_1} \right) \right) \quad (2.6)$$

to accommodate the model behavior in the high body bias regime, which is important in PD SOI. The parameter *Ketas* acts like an effective increment of the surface potential, which can be used to adjust the A_{bulk} rollup with the body potential V_{bsh}. While the other parameter *Keta* is used to tune the rate of rollup with V_{bsh}. By using this new expression, the non-physical drain current roll-off due to the dramatic A_{bulk} rollup at high body bias can be avoided [20].

2.4. Asymmetric and Bias-Dependent Source/Drain Resistance Model

BSIMSOI4.0 models source/drain resistances in two components: bias-independent diffusion resistance (sheet resistance) and bias-dependent LDD resistance. Accurate modeling of the bias-dependent LDD resistances is important for deep submicron CMOS technologies. In BSIMSOI3.2 and BSIMPD models, the LDD source/drain resistance R_{ds}(V) is modeled internally through the I-V equation and symmetry is assumed for the source and drain sides. BSIMSOI4.0 keeps this option for the sake of simulation efficiency. In addition, BSIMSOI4.0 allows the source LDD resistance R_s(V) and the drain LDD resistance R_d(V) to be external and asymmetric (i.e. R_s(V) and R_d(V) can be connected between the external and internal source and drain nodes, respectively; furthermore, R_s(V) does not have to be equal to R_d(V)). This feature makes accurate RF CMOS simulation possible. The internal R_{ds}(V) option can be invoked by setting the model selector ***rdsMod*** = 0 (**interna**l) and the external one for R_s(V) and R_d(V) by setting ***rdsMod*** = 1 (**external**).

• ***rdsMod*** = 0 (Internal *Rds*(V))

$$R_{ds} = R_{dsw} \frac{1 + P_{rwg} V_{gsteff} + P_{rwb}\left(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}\right)}{\left(10^6 W_{eff}^{'}\right)^{Wr}}$$

• ***rdsMod*** = 1 (External *Rd*(V) and *Rs*(V))

$$R_d(V) = \frac{RDWMIN + RDW \cdot \left[-PRWB \cdot V_{bd} + \dfrac{1}{1 + PRWG \cdot (V_{gd} - V_{fbsd})}\right]}{\left(1e6 \cdot W_{eff}\right)^{WR} \cdot NF}$$

$$R_s(V) = \frac{RSWMIN + RSW \cdot \left[-PRWB \cdot V_{bs} + \dfrac{1}{1 + PRWG \cdot (V_{gs} - V_{fbsd})}\right]}{\left(1e6 \cdot W_{eff}\right)^{WR} \cdot NF}$$

where $V_{fbsd} = \dfrac{k_B T}{q} \ln\left(\dfrac{N_{gate}}{10^{20}}\right)$ for NGATE larger than 0, otherwise $V_{fbsd} = 0$.

2.5. Single Drain Current Equation

After improving the V_{th} and A_{bulk} behavior in the high body bias regime, we can describe the MOSFET drain current by the same equation as BSIM3v3. The effective drain voltage V_{dseff} and effective gate overdrive voltage V_{gsteff} introduced in BSIM3v3 [1] are employed to link subthreshold, linear and saturation operation regions into a single expression as

$$I_{ds,MOSFET} = \frac{I_{ds0}}{1 + \dfrac{R_{ds} I_{dso}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)$$

$$\beta = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}}$$

$$I_{dso} = \frac{\beta V_{gsteff}\left(1 - A_{bulk} \dfrac{V_{dseff}}{2\left(V_{gsteff} + 2v_t\right)}\right) V_{dseff}}{1 + \dfrac{V_{dseff}}{E_{sat} L_{eff}}} \tag{2.7}$$

where R_{ds} is the source/drain series resistance, μ_{eff} is the mobility, E_{sat} is the critical electrical field at which the carrier velocity becomes saturated and V_A accounts for channel length modulation (CLM) and DIBL as in BSIM3v3. The substrate current body effect (SCBE) [8, 9] on V_A is not included because it has been taken into account explicitly by the real floating body simulation determined by the body currents, which will be detailed in the next chapter.