Chapter 4: MOS C-V Model

BSIMPD approaches capacitance modeling by adding SOI-specific capacitive effect to the C-V model of BSIM3v3. Similar to the I-V case, the body charges belonged to the floating body node will be our emphasis. The model incorporates features listed below with the SOI-specific features bold-faced and italicized.

- Separate effective channel length and width for IV and CV models.
- The CV model is not piece-wise (i.e. divided into inversion, depletion, and accumulation). Instead, a single equation is used for each nodal charge covering all regions of operation. This ensures continuity of all derivatives and enhances convergence properties. Just like in BSIM3v3, the inversion and body capacitances are continuous at the threshold voltage.
- Threshold voltage formulation is consistent with the IV model. Body effect and DIBL are automatically incorporated in the capacitance model.
- Intrinsic capacitance model has two options. The capMod = 2 option yields capacitance model based on BSIM3v3 short channel capacitance model. The capMod = 3 option is the new charge-thickness model from BSIM3v3.2 [4].
- Front gate overlap capacitance is comprised of two parts: 1) a bias independent part which models the effective overlap capacitance between the gate and the heavily doped source/drain, and 2) a gate bias dependent part between the gate and the LDD region.
- Bias independent fringing capacitances are added between the gate and source as well as the gate and drain. ***A sidewall source/drain to substrate (under the buried oxide) fringing capacitance is added.***
- ***A source/drain-buried oxide-Si substrate parasitic MOS capacitor is added.***
- ***Body-to-back-gate coupling is added.***

A good intrinsic charge model is important in bulk MOSFETs because intrinsic capacitance comprises a sizable portion of the overall capacitance, and because a well behaved charge model is required for robust large circuit simulation convergence. In analog applications there are devices biased near the threshold voltage. Thus, a good charge model must be well-behaved in transition regions as well. To ensure proper behavior, both the I-V and C-V model equations should be developed from an identical set of charge equations so that C_{ij}/I_d is well behaved.

A good physical charge model of SOI MOSFETs is even more important than in bulk. This is because transient behavior of the floating body depends on capacitive currents [18]. Also, due to the floating body node, convergence issues in PD SOI are more volatile than in bulk, so that charge smoothness and robustness are important. An example is that a large negative guess of body potential by SPICE during iterations can force the transistor into depletion, and a smooth transition between depletion and inversion is required. Therefore the gate/source/drain/backgate to body capacitive coupling is important in PD SOI.

4.1. Charge Conservation

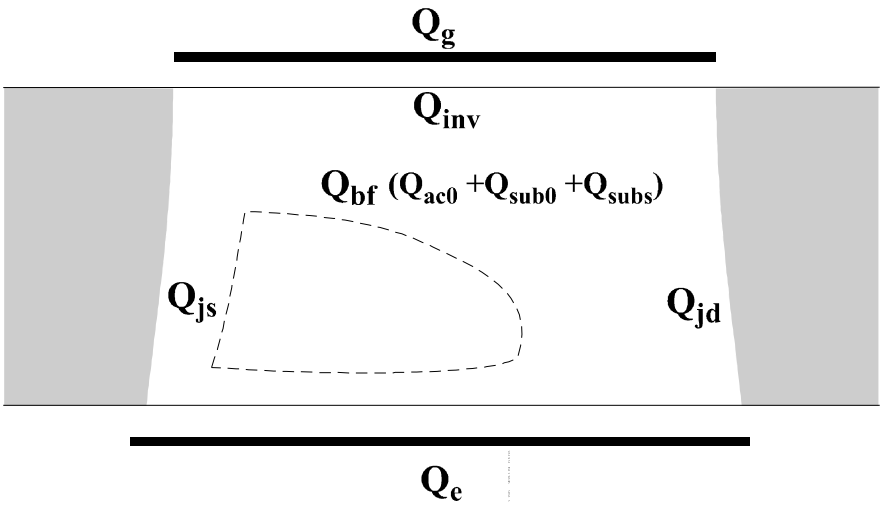

Fig. 4.1 Intrinsic charge components in BSIMPD CV model

To ensure charge conservation, terminal charges instead of terminal voltages are used as state variables. The terminal charges Q_g, Q_d, Q_s, Q_b, and Q_e are the charges associated with the **g**ate, **d**rain, **s**ource, **b**ody, and substrat**e** respectively. These charges can be expressed in terms of inversion charge (Q_{inv}), front gate body charge (Q_{Bf}), source junction charge (Q_{js}) and drain junction charge (Q_{jd}). The intrinsic charges are distributed between the nodes as shown in Fig. 4.1. The charge conservation equations are:

$$\begin{aligned}
Q_{Bf} &= Q_{ac0} + Q_{sub0} + Q_{subs} \\
Q_{inv} &= Q_{inv,s} + Q_{inv,d} \\
Q_g &= -\left(Q_{inv} + Q_{Bf}\right) \\
Q_b &= Q_{Bf} - Q_e + Q_{js} + Q_{jd} \\
Q_s &= Q_{inv,s} - Q_{js} \\
Q_d &= Q_{inv,d} - Q_{jd} \\
Q_g + Q_e + Q_b + Q_s + Q_d &= 0
\end{aligned} \tag{4.1}$$

The front gate body charge (Q_{Bf}) is composed of the accumulation charge (Q_{ac0}) and the bulk charge (Q_{sub0} and Q_{subs}), which may be divided further into two components: the bulk charge at V_{ds}=0 (Q_{sub0}), and the bulk charge induced by the drain bias (Q_{subs}) (similar to δQ_{sub} in BSIM3v3).

All capacitances are derived from the charges to ensure charge conservation. Since there are 5 charge nodes, there are 25 (as compared to 16 in BSIM3v3) components. For each component: $C_{ij} = \frac{dQ_i}{dV_j}$, where *i* and *j* denote transistor nodes. In addition, $\sum_i C_{ij} = \sum_j C_{ij} = 0$.

4.2. Intrinsic Charges

BSIMPD uses similar expressions to BSIM3v3 for Q_{inv} and Q_{Bf}. First, the bulk charge constant A_{bulkCV} is defined as

$$A_{bulkCV} = A_{bulk0}\left(1+\left(\frac{CLC}{L_{active}}\right)^{CLE}\right) \tag{4.2}$$

where

$$A_{bulk0} = A_{bulk}\left(V_{gsteff}=0\right) \tag{4.3}$$

This is done in order to empirically fit V_{dsatCV} to channel length. Experimentally,

$$V_{dsatIV} < V_{dsatCV} < V_{dsatIV}\big|_{L\to\infty} = \frac{V_{gsteffCV}}{A_{bulk}} \tag{4.4}$$

The effective CV V_{gst} is defined as

$$V_{gsteffCV} = nv_t \ln\left(1+\exp\left[\frac{V_{gs}-V_{th}}{nv_t}\right]\right) \tag{4.5}$$

Then we can calculate the CV saturation drain voltage

$$V_{dsatCV} = V_{gsteffCV} \,/\, A_{bulkCV}\,. \tag{4.6}$$

Define effective CV V_{ds} as

$$V_{dsCV} = V_{dsatCV} - \frac{1}{2}(V_{dsatCV} - V_{ds} - \delta + \sqrt{(V_{dsatCV} - V_{ds} - \delta)^2 + 4\delta V_{dsatCV}}) \tag{4.7}$$

Then the inversion charge can be expressed as

$$Q_{inv} = -W_{active}L_{active}C_{ox}\left(\left(V_{gsteffCV} - \frac{A_{bulkCV}}{2}V_{dsCV}\right) + \frac{A_{bulkCV}{}^2 V_{dsCV}{}^2}{12\left(V_{gsteffCV} - \frac{A_{bulkCV}{}^2}{2}V_{dsCV}\right)}\right) \tag{4.8}$$

where W_{active} and L_{active} are the effective channel width and length in CV, respectively. The channel partition can be set by the *Xpart* parameter. The exact evaluation of source and drain charges for each partition option is presented in Appendix C.

A parameter V_{FBeff} is used to smooth the transition between accumulation and depletion regions. The expression for V_{FBeff} is:

$$V_{FBeff} = V_{fb} - 0.5\left(\left(V_{fb} - V_{gb} - \delta\right) + \sqrt{\left(V_{fb} - V_{gb} - \delta\right)^2 + \delta^2} \right) \tag{4.9}$$

where $V_{gb} = V_{gs} - V_{bseff}$, $V_{fb} = V_{th} - \phi_s - K_{1eff}\sqrt{\phi_s - V_{bseff}}$.

The physical meaning of the function is the following: it is equal to V_{gb} for $V_{gb}<V_{FB}$, and equal to V_{FB} for $V_{gb}>V_{FB}$. Using V_{FBeff}, the accumulation charge can be calculated as

$$Q_{ac0} = -F_{body} W_{active} L_{activeB} C_{ox} (V_{FBeff} - V_{fb}) \tag{4.10}$$

where $L_{activeB} = L_{active} - DLCB$. Notice that the parameters F_{body} and $DLCB$ are provided to give a better fit for the SOI-specific history dependence of the body charge [14].

The gate-induced depletion charge and drain-induced depletion charge can be expressed as

$$Q_{sub0} = -F_{body} W_{active} L_{activeB} C_{ox} \frac{{K_{1eff}}^2}{2} \left(-1 + \sqrt{1 + \frac{4(V_{gs} - V_{FBeff} - V_{gsteffCV} - V_{bseff})}{{K_{1eff}}^2}} \right) \tag{4.11}$$

$$Q_{subs} = F_{body} W_{active} L_{activeB} K_{1eff} C_{ox} \left(1 - A_{bulkCV}\right) \left[\frac{V_{dsCV}}{2} - \frac{A_{bulkCV} V_{dsCV}^2}{12\left(V_{gsteffCV} - A_{bulkCV} V_{dsCV}/2\right)} \right] \tag{4.12}$$

respectively.

Finally, the back gate body charge can be modeled by

$$Q_e = F_{body} W_{active} L_{activeBG} C_{box} \left(V_{es} - V_{fbb} - V_{bseff}\right) \tag{4.13}$$

where $L_{activeBG} = L_{activeB} + 2\delta L_{bg}$. The parameter δL_{bg} is provided to count the difference of $L_{activeB}$ and $L_{activeBG}$ due to the source/drain extension in the front channel.

For capMod=3, the flat band voltage is calculated from the bias-independent threshold voltage, which is different from capMod=2. For the finite thickness formulation, refer to Chapter 4 of BSIM3v3.2 Users' Manual.

4.3. Source/Drain Junction Charges

Beside the junction depletion capacitance considered in BSIM3v3, the diffusion capacitance, which is important in the forward body-bias regime [20], is also included in BSIMPD. The source/drain junction charges Q_{jswg} / Q_{jdwg} can therefore be expressed as

$$\begin{aligned} Q_{jswg} &= Q_{bsdep} + Q_{bsdif} \\ Q_{jdwg} &= Q_{bddep} + Q_{bddif} \end{aligned} \tag{4.14}$$

The depletion charges Q_{bsdep} / Q_{bddep} have similar expressions as in BSIM3v3 [Appendix C]. While the diffusion charges Q_{bsdif} / Q_{bddif} can be modeled by

$$\begin{aligned} Q_{bsdif} &= \tau \frac{W_{eff}'}{N_{seg}} T_{si} J_{sbjt} \left[1 + L_{dif0} \left(L_{bj0} \left(\frac{1}{L_{eff}} + \frac{1}{L_n} \right) \right)^{N_{dif}} \right] \left[\exp\left(\frac{V_{bs}}{n_{dios} V_t} \right) - 1 \right] \frac{1}{\sqrt{E_{hlis} + 1}} \\ Q_{bddif} &= \tau \frac{W_{eff}'}{N_{seg}} T_{si} J_{dbjt} \left[1 + L_{dif0} \left(L_{bj0} \left(\frac{1}{L_{eff}} + \frac{1}{L_n} \right) \right)^{N_{dif}} \right] \left[\exp\left(\frac{V_{bd}}{n_{diod} V_t} \right) - 1 \right] \frac{1}{\sqrt{E_{hlid} + 1}} \end{aligned} \tag{4.15}$$

The parameter τ represents the transit time of the injected minority carriers in the body. The parameters L_{dif0} and N_{dif} are provided to better fit the data.

4.4. Extrinsic Capacitances

Expressions for extrinsic (parasitic) capacitances that are common in bulk and SOI MOSFETs are taken directly from BSIM3v3. They are source/drain-to-gate overlap capacitance and source/drain-to-gate fringing capacitance. Additional SOI-specific parasitics added are substrate-to-source sidewall capacitance C_{essw}, and substrate-to-drain sidewall capacitance C_{edsw}, substrate-to-source bottom capacitance (C_{esb}) and substrate-to-drain bottom capacitance (C_{edb}) [Fig. 4.2].

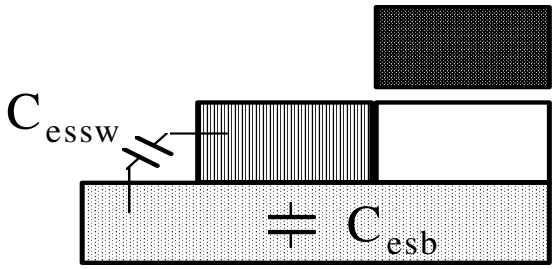

Fig. 4.2 SOI MOSFET extrinsic charge components. C_{essw} is the substrate-to-source sidewall capacitance. C_{esb} is the substrate-to-source bottom capacitance.

In SOI, there is a parasitic source/drain-buried oxide-Si substrate parasitic MOS structure with a bias dependent capacitance. If $V_{s,d}$=0, this MOS structure might be in accumulation. However, if $V_{s,d}$=V_{dd}, the MOS structure is in depletion with a much smaller capacitance, because the Si substrate is lightly doped. The bias dependence of this capacitance is similar to high frequency MOS depletion capacitance as shown in Fig. 4.3. It might be substantial in devices with large source/drain diffusion areas. BSIMPD models it by piece-wise expressions, with accurately chosen parameters to achieve smoothness of capacitance and continuity to the second derivative of charge. The substrate-to-source bottom capacitance (per unit source/drain area) C_{esb} is:

$$C_{esb} = \begin{cases} C_{box} & if \quad V_{se} < V_{sdfb} \\ C_{box} - \dfrac{1}{A_{sd}}\left(C_{box} - C_{\min}\right)\left(\dfrac{V_{se} - V_{sdfb}}{V_{sdth} - V_{sdfb}}\right)^2 & elseif \quad V_{se} < V_{sdfb} + A_{sd}\left(V_{sdth} - V_{sdfb}\right) \\ C_{\min} + \dfrac{1}{1 - A_{sd}}\left(C_{box} - C_{\min}\right)\left(\dfrac{V_{se} - V_{sdth}}{V_{sdth} - V_{sdfb}}\right)^2 & elseif \quad V_{se} < V_{sdth} \\ C_{\min} & else \end{cases} \tag{4.16}$$

Physical parameters V_{sdfb} (flat-band voltage of the MOS structure) and V_{sdth} (threshold voltage of the MOS structure) can be easily extracted from measurement. C_{min} should also be extracted from measurement, and it can account for deep depletion as well. A_{sd} is a smoothing parameter.

The expression for C_{edb} is similar to C_{esb}. Fig. 4.3 shows the comparison of the model and measured C_{esb}.

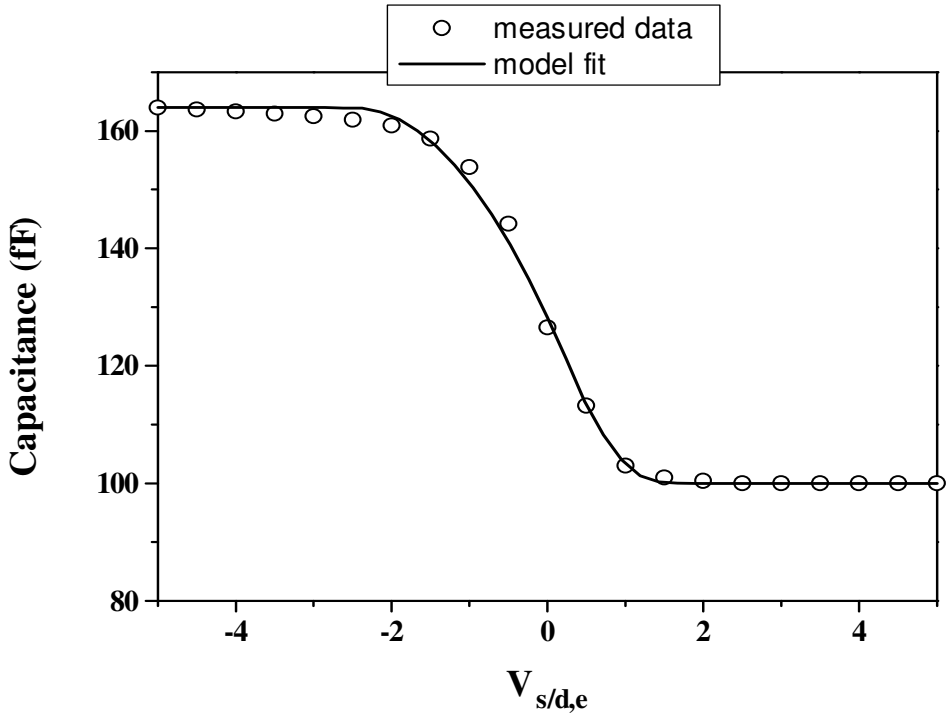

Fig. 4.3 Bottom source/drain to substrate capacitance for a PD SOI MOSFET.

Finally, the sidewall source/drain to substrate capacitance (per unit source/drain perimeter length) can be expressed by

$$C_{s/d,esw} = C_{sdesw} \log\left(1 + \frac{T_{si}}{T_{box}}\right) \tag{4.17}$$

which depends on the silicon film thickness T_{si} and the buried oxide thickness T_{box}. The parameter C_{sdesw} represents the fringing capacitance per unit length.

4.5. Body Contact Parasitics

The parasitic capacitive coupling due to the body contact is considered in BSIMPD. The

instance parameter A_{gbcp} represents the parasitic gate-to-body overlap area due to the body contact, and A_{ebcp} represents the parasitic substrate-to-body overlap area. The effect may be significant for small area devices [CV part in Appendix C].