BSIMSOIv4.4

BSIM Group

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BSIM SOI Bug Fixes and Enhancements

NF Scaling of Rds

Issue: Bug in TNOI Model = 0 **file: b4soinoi.c line: 366**

```
switch( model->B4SOItnoiMod )
{
case 0:
      NevalSrc(&noizDens[B4SOIIDNOIZ],
          &lnNdens[B4SOIIDNOIZ], ckt,
          THERMNOISE,
          here->B4SOIdNodePrime,
          here->B4SOIsNodePrime,
          (here->B4SOIueff
          * FABS(here->B4SOIqinv
                / (pParam->B4SOIleff
                * pParam->B4SOIleff
                + here->B4SOIueff*FABS
                  (here->B4SOIqinv)
                *  here->B4SOIrds)))
                *  tempRatioSH
                * model->B4SOIntnoi );
```

here->B4SOIqinv is scaled by NF, while here->B4SOIrds is not

NF Scaling of Rds

Bug-fix: **here->B4SOIrds is scaled by NF.**

Previous code: **File: b4soild.c** **line: 2820**

here->B4SOIrds = Rds;

Modification:

here->B4SOIrds = Rds/here->B4SOInf;

Reported By: Lawrence Wagner, IBM

Negative ‘rdsw’ and ‘rds0’

Negative ‘rdsw’ and ‘rds0’:

- **The implementation of ‘rdsw’ and ‘rds0’ checks are different in C code and VA**
- **The VA code does not allow negative ‘rdsw’ and ‘rds0’ while C code does**
- **C code does the check in only PARAMCHK = 1, Verilog-A does in both**
- **QA test is done in PARAMCHK=0**

```
if (pParam->B4SOIrdsw < 0.0)        {
fprintf(fplog, "Warning: Rdsw = %g is negative. Set to zero.\n",
                pParam->B4SOIrdsw);
printf("Warning: Rdsw = %g is negative. Set to zero.\n",
pParam->B4SOIrdsw);
pParam->B4SOIrdsw = 0.0;
pParam->B4SOIrds0 = 0.0;
```

File: b4soicheck.c lines: 521

Negative ‘rdsw’ and ‘rds0’

Considerations:

- **ADI and IBM expressed concern about allowing negative ‘rdsw’ and ‘rds0’**
- **IBM would like to see identical results irrespective of ‘PARAMCHK’ value**
- **Last CMC meeting all agreed to implement the above features**

Modification:

- **According to CMC’s recommendation the check is implemented irrespective of ‘PARAMCHK’; C and VA codes behave identical**

Vb blow up in SOIMOD=2

- b4soild.c line 2150:
- Vbs0 is evaluated as (BSIMSOIv 4.3 manual: Page 50)

$$V_{bs0} = \frac{C_{Si}}{C_{Si} + C_{BOX}} \cdot \left(phi - \frac{qN_{ch}\left(1 + N_{LX}/L_{eff}\right)}{2\varepsilon_{Si}} \cdot T_{Si}^{\,2} + V_{nonideal} + \Delta V_{DIBL} \right) + \eta_e \frac{C_{BOX}}{C_{Si} + C_{BOX}} \cdot \left(V_{es} - V_{FBb}\right)$$

where $C_{Si} = \frac{\varepsilon_{Si}}{T_{Si}}, C_{BOX} = \frac{\varepsilon_{OX}}{T_{BOX}}, C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}}$

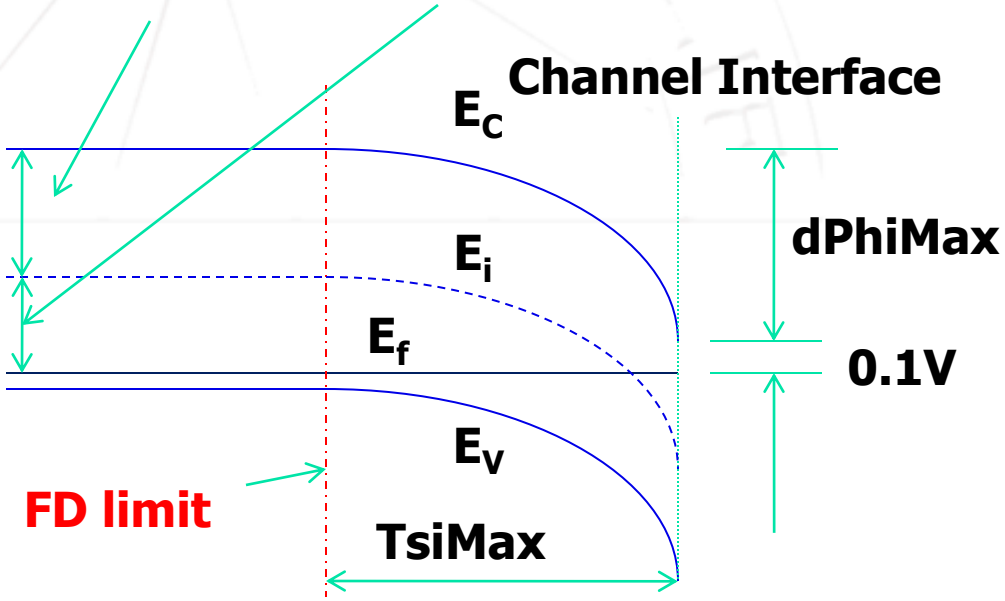
- The highlighted term is Qsi/(2*Csi)
- High values of Nch / Tsi combination causes un-relistic Vbs values (-50V)

Check needed on Band Bending

- Maximum allowed band bending and N_{ch}/T_{si} limit in SOIMOD=2:

$$dPhi_{Max} = \frac{E_g}{2q} - 0.1 + \frac{kT}{q}\ln\left(\frac{N_{ch}}{n_i}\right)$$

$$dPhi_{Max} \approx \left(\frac{E_g}{q} - 0.1\right)\cdot V$$



Implemented Correction

- If $\frac{qN_{ch}\left(1+N_{LX}/L_{eff}\right)}{2\varepsilon_{Si}}\cdot T_{Si}^{2}$ exceeds dPhiMax in

  SOIMOD=2, set Nch=NchMax, where:

$$N_{ch\max}=\frac{dPhi_{Max}\cdot 2\varepsilon_{Si}}{q\cdot T_{Si}^{2}\cdot\left(1+N_{lx}/L_{eff}\right)}$$

- This check applies to SOIMOD=2 only.
- An warning is issued to the user.
- File: b4soiset.c (line:2173)

Enhancement of Fringe Capacitance

IBM's request for enhanced sidewall fringe capacitance formulation (CMC Action item 10Q3.13):

Current code:

csesw = csdesw*ln(1+Tsi/Tbox) (b4soitemp.c line: 1670)

IBM proposal: csesw = csdesw*ln[2*(1+Tsi/Tbox)]

Implemented: csesw = csdesw*ln[Cfrcoeff*(1+Tsi/Tbox)]

Here Cfrcoeff (new model parameter) is given a default value = 1 for backward compatibility and a maximum limit of 2.

Temperature Derivative Fixes

- In SOIMOD=1 and 2, extensive derivative fixes are provided by Lawrence Wagner and Calvin Bittner. Please check the file ‘BSIMSOIv4.4_Derivative_Fixes’ for details.